What is claimed is:

1. A flash ROM management apparatus, comprising:

a storage device capable of storing a plurality of address records, each address record comprising an identity and an address range associated with a flash ROM;

a strapping component, configured to output a signal to determine flash ROM type; and

a process unit, coupled to the storage device and the strapping component, receiving a memory access request with an access range from the CPU and the signal, determining the flash ROM type according to the signal, querying the identity by matching the access range and the address range, and executing an LPC 1.1 memory access instruction with the identity and the access range corresponding to the memory cycle.

2. The apparatus as claimed in claim 1 wherein the identity is an "IDSEL" number associated with a firmware hub flash ROM.

3. The apparatus as claimed in claim 1 wherein the address range is a pair comprising a base address and an end address.

4. The apparatus as claimed in claim 1 wherein the address range is a pair comprising a base address and memory size.

5. The apparatus as claimed in claim 1 wherein the flash ROM type is an LPC flash ROM or a firmware hub flash ROM.

6. The apparatus as claimed in claim 1 wherein the memory access request is a memory read request or a memory write request.

7. The apparatus as claimed in claim 1 wherein, in the process unit, the LPC 1.1 memory access instruction is an LPC memory read instruction or an LPC memory write instruction, and the LPC memory read instruction or the LPC memory write instruction corresponds to the LPC memory cycle.

8. The apparatus as claimed in claim 1 wherein, in the process unit, the LPC 1.1 memory access instruction is a firmware hub memory read instruction or a firmware hub memory write instruction, and the firmware hub memory read instruction or the firmware hub memory write instruction corresponds to the firmware hub memory cycle.

9. The apparatus as claimed in claim 1 wherein a basic input/output system (BIOS) flag within the address record indicates whether the system BIOS is stored in flash ROM.

10. The apparatus as claimed in claim 9 further comprising a configuration unit detecting an error message indicating system BIOS failure, and resetting the BIOS flag for further reboot.

11. A method of flash ROM management, comprising using a computer to perform the steps of:

receiving a memory access request with an access range from a CPU;

receiving a signal output from a strapping component to determine flash ROM type;

inputting a plurality of address records associated with a flash ROM, wherein the address record comprises an identity and an address range;

querying the identity by matching the access range and the address range; and

executing an LPC 1.1 memory access instruction with the access range and identity corresponding to the memory cycle.

12. The method as claimed in claim 11, wherein the memory access request is a memory read request or a memory write request.

13. The method as claimed in claim 11, wherein the signal determines whether an LPC flash ROM or a firmware hub flash ROM is present.

14. The method as claimed in claim 11, wherein the identity is an "IDSEL" number associated with a firmware hub flash ROM.

15. The method as claimed in claim 11, wherein the address range is a pair comprising a base address and end address.

16. The method as claimed in claim 11, wherein the address range is a pair comprising a base address and memory size.

17. The method as claimed in claim 11, wherein, in the step of executing an LPC 1.1 memory access instruction with the access range and the identity corresponding to memory cycle, the LPC 1.1 memory access instruction is an LPC memory read instruction or an LPC memory write instruction corresponding to LPC memory cycle.

18. The method as claimed in claim 11, wherein, in the step of executing an LPC 1.1 memory access instruction with the access range and the identity corresponding to memory cycle, the LPC 1.1 memory access instruction is a firmware hub memory read instruction or a firmware hub memory write instruction corresponding to the firmware hub memory cycle.